L2 Review - Introduction

A somewhat personal view of L2 from a former (yeah!) Trigger Leader

Outline:

- Why are we here? Motivations for review.
- Brief History: Design to commissioning of trigger.
- Issues to Consider: What I think you should consider and look for in other presentations.
- Conclusions: Four examples of possible committee conclusions.

Introduction – Why are we here?

- L2 Decision System has not yet at Run 2A baseline:
  - ➢L1A = 45 kHz L1A (10kHz), L2A = 300Hz (really DAQ spec), Rejection=150 (50)
  - ➢Multiple Alphas, Muon Interface Board
  - ➢Construction and Commissioning of system has been very difficult:
    - Many interface board designs to commission
    - Unexpected technical problems: bad vias, Mbus arbitration
    - Loss of peopple (eg Ron Moore from μ–Interface to TDCs)
    - Huge effort to commission system: >15 people, >30 person-years
- Can 2A baseline be achieved in a finite period of time?
  - ➢Limitations from external issues (SVX readout, SVT processing)

Why are we here?

- What is the 2B baseline spec?
  - L1A=45kHz, L2A=1kHz Þ less rejection
  - More occupancy/crossing and High Pt Triggers larger fraction of L1A (and possibly more fake occupancy)
    Þ more complicated events and algorithms
  - Smaller fraction of L1A require SVT at L2 (90% Þ 20%)
    Þ new tricks may increase capabilities
- Even if 2A baseline is achieved, can we achieve the baseline operation with the 2B occupancies?
- Is the system robust/reliable enough to operate until the end of 2B (2008-2009)

Introduction – Why review NOW?

- Directors/Lehman review schedules dictate that we define the baseline for 2B upgrades NOW. We must define a single baseline plan. This cannot include options for several different solutions.
- This is good because it forces us to seriously consider what direction to take for the next 5-6 years. If we wait another year, inertia will dictate the plan.

Brief History - Trigger Design

1992-93 "Deadtimeless" Trigger/DAQ proposed

1995 Front-end/Trigger Base-lined including L1CAL, XFT, XTRP, L1Muon, ClusterFinder, SVT, L1 and L2 Decision systems

1995 1st FE/DAQ/Trigger Workshop – FNAL

1996 2nd FE/DAQ/Trigger Workshop – Michigan

1997 3rd FE/DAQ/Trigger Workshop – Michigan

1998 1st and 2nd Joint CDF/D0 L2 Workshops – FNAL/Michigan

1999 4th FE/DAQ/Trigger Workshop – UCLA

Brief History: Trigger Installation at B0 (Plan after '99 UCLA Workshop)

Test at B0 with				
prototype/pre-prod	First 50%		Last 50%	installed

Calendar Month

Subsystem	99												00		Actual Commission	
	2	3	4	5	6	7	8	9	10	11	12		1	2	First	Comp.
Lv1 Calorimeter															Dec-99	Oct-00
Lv2 Calorimeter															Apr-01	Oct-01
CMU trigger															Sep-00	May-01
CMP trigger															May-02	Jun-02
XFT															Sep-00	Oct-00
XTRP															Oct-00	Aug-01
Lv1 Decision															Dec-99	Oct-00
Lv2 Decision															Apr-01	May-02
SVT															May-01	Sep-01
EVB & L3 trigger																

Brief History: Commissioning Milestones '99-'01

12/15/99 L1 Cal & L1 Dec installed, Trigger on Cosmics

8/00 XFT, Muon Trigger Installed (μ-cosmics)

10/00 Comm. Run: L1 Jets, γ, μ-stub, CLC, (XFT/XTRP) & L3

4/01 Begin Run 2: Add XTRP - L1 electron, CMU+track & L3

Clusters in CF (not triggered until late 9/01)

5/01 Tracks in SVT (not triggered until late 9/01)

6-7/01 L1 CMP/CMX Muons

8/01 L1 Two Track Triggers (XTRP synch and via problems)

4-9/01 L2: Struggle with Mbus arbitration, Alpha via problems, interface board commissioning, cluster finder synch problems.

Can't do PIO (needed for Reces)

A Brief History: Sept 2001 Workshop

Scheduled workshop with Goal of cutting at L2 before Oct '01.
Set the following goals at end of workshop:

- Before Oct Shutdown (green – achieved, red – not):
  - Artificial MB delays to work around arbitration
  - Cut on Jets, SVT tracks, Electrons (Jan '02).
- During Shutdown: test New MB backplane (Feb '02)
- By Jan 1 '02: 4 Alphas + all interface (except muon)
- Trigger SPLs (Ristori and Wilson) establish plan for new L2 Teststand hardware
  - Provide individual board (system?) testing w/o CDF as pulse generator.
  - L2 Pulsar as data source and Magical Mystery Board as Magic bus analyzer
- Plan for Review of system status before end of the year

Brief History: Sept 2001 Workshop

Trigger SPLs (Ristori and Wilson) consider risk of failure of baseline system to be non-negligible.
Therefore pursue backup plans:

- Tested backup solution cutting on SVT tracks (9/19/01):
  - GhostBuster (GB)⇔TS (bypass L2Dec) before route through SVTlist is fully functional. Provides very useful testbed for SVX/SVT/TS tests through Dec '01
  - Prepare to Run after shutdown w/ Alpha cutting on jets and GB cutting on SVT tracks. Not needed since baseline system worked.
- Future Backup solutions considered:
  - Magical Mystery Board to readout Interface boards and feed all data into TRACKlist boards on Mbus. Only one type of Interface doing MagicBus arbitration. Mbus works with delays – not pursued.
  - MMB to readout RECES and push sparsified data into TRACKlist. PIO made to work – not pursued.
  - Longer term: replacement of MBus, interface modules, with "Universal" interface design and "standard" serial link (eg SVT cable or CERN SLINK) based on L2 Pulsar (See Ted's Talk). Not pushed past basic concept since existing system continued to progress.

Brief History: Dec 2001 Review

- Improve operations support before start of Physics running in Jan ‘02
  - ➢ Pager rotation started early Jan ‘02, daily report to L2 Mailing list
- Address lack of sufficient spares: making additional ISO boards, work on fixing CLIST
- Set timetable for Mbus test decisions and review (by Mar 1) to be ready for 5E31 in summer ’02
- Push for speedier software development:
  - ➢ New Trigger Software Czar (Peter Wittich just replaced by Tom Wright)
- Recommend construction of L2 Pulsar for test-stand. Request further review with Trigger group involving L2 experts
  - ➢ Presentations/Discussion in Feb, Apr, May, June at Trigger Hardware meetings
  - ➢ Mini-review of board 24 July, release prototype production early Aug

Brief History: Milestones 2002 and Beyond

Jan. Electron and γ-Iso Cutting. PIO problem solved RECES commissioning resumes (Cut in Physics Table early May)

Feb PECL arbitration abandoned, TTL arbitration tests until May

- PAL in socket glued to each board w/~10 blue wires. Last batch of Alpha's and μ-Interface have TTL on PCB.

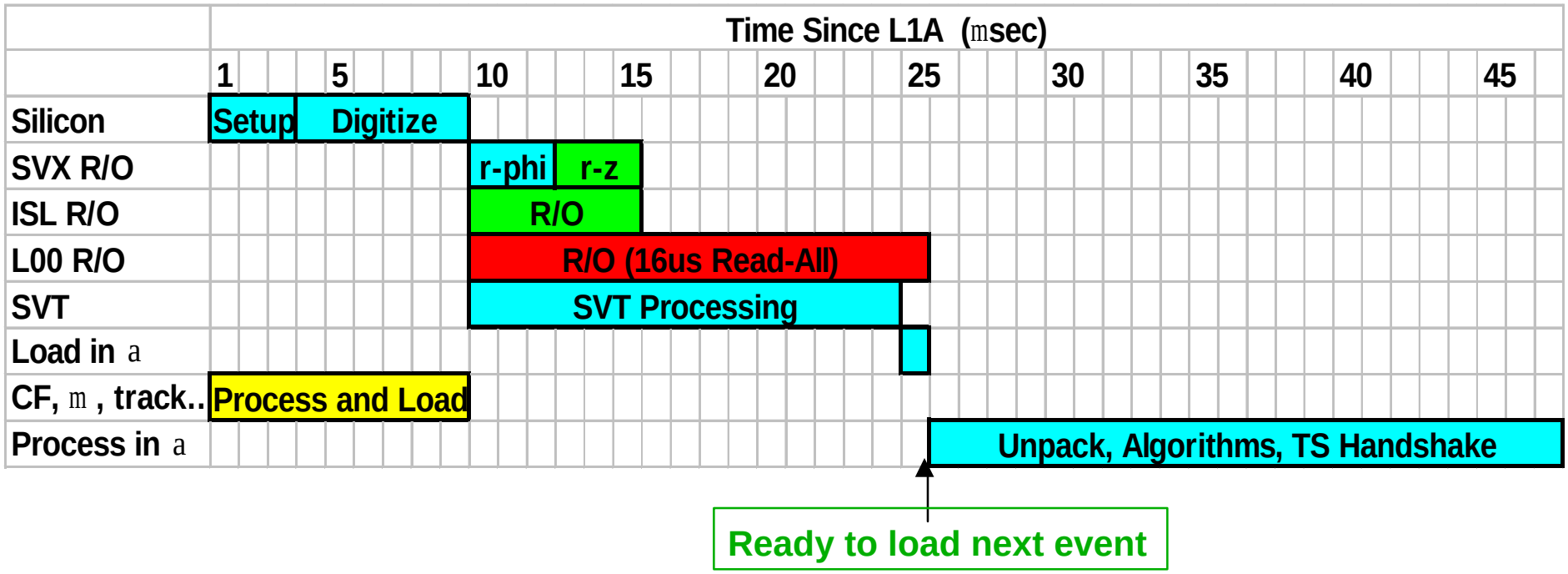
May TTL arbitration used for Physics since Early May

- Use "minimal" delays (CLIST – 400ns, XTRPlist – 1μsec, SVTlist – 1μsec) . Are delays needed? If so why? What affect do they have?

??? Multiple Alphas – Only tested data loading (Successful?). Are they needed to meet baseline performance?

??? Muon Interface – Needed for L>4-5x10^{31}, Muon triggers make up 40-45% of the L2 accept rate. Changes to L1 configuration could get us to 8x10^{31} . Delivery to B0 predicted to be in a few months for a couple of years.

Issues to Consider: Current L2 Timing



Loading time = SVX+SVT~25μs

Execution time ~ 22μs

L00 Digi+R/O = 25μs (read-all)

⇒ L1A limited to ~20kHz

Issues to Consider: Current Rate Limits

- Need to push on timing of Si readout, SVT, and L2 Decision. L2 should not assume that Si and SVT will not improve.
  - We can probably get to 30kHz, 40kHz will be very challenging
  - We should assume that DOIM problem will be solved and 12kHz rev-limit will be lifted
- L2 Decision Optimization
  - Test L2 independently → use SVT fake tracks to avoid slow SVX/SVT and L00.
  - Optimize Alpha code/firmware further.
  - For Run 2B, try new ideas like Early L2 decisions for events not requiring SVT (up from 10% to 80% of L1As). This can be done by reprogramming firmware within SVT too look at L1 bits and ignore events where SVT will not be needed. SVT would immediately (few μsec) send End Event to SVTlist.

Issues to Consider: SVX/SVT Timing

- SVT timing relies on prompt arrival of r-phi hits from SVX
  - Tweak overhead… may be able to squeeze 1μsec
  - Go from 8bit to 7bit digitization saves ~2.5μsec ⇒ interaction with ISL
  - Optimize SVX sparsification cuts ?? μsec
  - Optimize SVT processing times ?? μsec
- Optimize SVX readout
  - L00 readout currently sets a limit to speed of system
  - Can speed up by switching to 7bit digitization (is this acceptable?)
  - Can ISL have 8 bit and SVX, L00 have 7 bit or are multiple SRCs needed for that?
  - Advantages to separating ISL, L00, SVX into different SRCs to allow SVT to start processing data from SVX earlier. This is lots of work for Si DAQ/TS experts. Should simulate to assess improvement.
  - Need to set priorities to improve bandwidth and find new experts to relieve the old in TSI and Si. This will not be easy or quick.

Issues to Consider: Evaluating the Existing System

- Performance of system:
  - Achievable L1A rate with deadtime < 10%
  - Rejection factor (probably not changed with a new system)
- Robustness/Reliability
  - Many interface boards that must be supported, spreads spares and expertise thin.
  - Most boards have glued chips and wires for TTL. Will these be reliable?
  - Boards based on old technology (also True of L1 and FE/DAQ).
  - Many boards difficult to debug since have no VME interface or no L2 buffers to allow readout of data. Exceptions are TRACKlist boards and Muon board
  - Are we prepared for the loss of any individual expert?
  - Are we prepared to maintain the system with drain to new expts (LHC)?
- Flexibility
  - Will the system be able to meet unexpected challenges in 2A or 2B?
  - If system meets spec, is there enough “headroom” for the unexpected (e.g. higher than anticipated track fake rates)?

Issues to Consider: Wish list for New Hardware

- As many commercially available/tested components as possible (eg Links)
- Faster processor with faster memory. Ability to upgrade processor easily.
  - L2 Beta project (D0) replaces Alpha with 9U adapter card for a Compact PCI single board computer. Beta Adapter board provides PCI ⇔ Mbus and PCI ⇔ VME. See Bob's talk.
  - Replacement system might use PC as processor
- Fewer interface board designs
  - Single design with capability to work with all L2 Input protocols (eg Hotlink, Taxi, SVT)
  - Design for testing with VME Interface including L2 readout buffers for reading out data as diagnostic readout. Like current TRACKlist, Muon designs
  - Ability to sink/source test data (e.g. SVT Spy Buffer)
- Remove 2-Stage Pipe requirement of existing system?
  - Allow decisions out of FIFO order?
  - Allow interface boards to be in different stages of the pipeline?
  - Use multiple processors to look at different events instead of different algorithms?

Conclusions

What might you conclude?

1. The existing system is fine for 2A and 2B, it would be a waste of time and manpower to replace it.
   - We drop L2 from the 2B Upgrade project
2. The existing system provided the needed bandwidth into the processors and the interface systems are sound. Alphas will be hard to maintain or are not fast enough.
   - Buy into the L2 Beta project. Identify a group to make a new version of Beta adapter card with LVDS connection to TS (D0 is ECL) and interface to CDF signals from P2 (eg CDF_CLK and L1A)

Conclusions (cont)

3. The existing looks like a disaster because it will never meet the rate requirement or is unmaintainable
   - Build a new system. Baseline for Lehman is something like Ted's proposal.
   - Call for detailed proposals to be evaluated by follow-up review in 3 months.
4. Not sure if existing system will do the job because bandwidth capability and requirements (eg occupancy) are not clear
   - Put new system in as Lehman Baseline
   - Committee recommends specific measurements be made to further explore system capabilities and project needs for 2B.
   - Follow-up review in 2 months to evaluate system performance and make final decision. Re-baseline as needed.